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EXAMINER

HUBER, ROBERT T

ART UNIT

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/531,141	<b>Applicant(s)</b> TRICOMI ET AL.	
	<b>Examiner</b> ROBERT HUBER	<b>Art Unit</b> 2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 August 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 2-8 and 13-25 is/are pending in the application.
- 4a) Of the above claim(s) 18-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-8, 13-17 and 22-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 December 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                       | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>10/28/2009</u> .  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 112***

1. The Examiner acknowledges the withdrawal of claims 18 – 21 filed on August 5, 2009. The rejection of claim(s) 8 – 12 under USC 112, first paragraph, cited in the previous office action filed on March 2, 2009 is (are) hereby withdrawn.

2. The Examiner acknowledges the amendment(s) to claims 16 and 17 filed on August 5, 2009. The rejection of claim(s) 2 – 8 and 13 – 17 under USC 112, second paragraph, cited in the previous office action filed on March 2, 2009 is (are) hereby withdrawn.

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 22 and 23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, the claims recite "*a height of at least one of the stamped pedestals is between 1/10 of a height of the carrier device to the height of the carrier device.*" However, there is no support in the specification for such a limitation. Rather, the specification supports a pedestal height "*may be*

*approximately in a range of from 1/5 to twice the material thickness h of the carrier device “ (page 15, and a similar recitation on page 13).*

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 2 – 7, 13, 14, 16, 17, and 22 - 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pritchard et al. (US 5,479,050, prior art of record) in view of Kwon et al. (US 5,365,409, prior art of record).

a. Regarding claim 16, **Pritchard discloses an integrated circuit** (e.g. figure 1), **comprising:**

**a semiconductor die** (die 11);

**a carrier device comprising a die paddle onto which the die is attached** (paddle 16, disclosed in col. 1, line 65, which is the portion of leadframe 10 under semiconductor die 11), **where a plurality of stamped pedestals** (pedestals 12 and 13, disclose in col. 1, lines 65 – 67 to be stamped) **are arranged on the carrier device exteriorly surrounding and adjacent to the die paddle** (e.g. as seen in figure 1, the pedestals 12 and 13 exteriorly surround and are adjacent to the top of the die paddle region under the semiconductor die 11), **where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure** (e.g. as seen in the figure, the carrier device, die paddle, and stamped pedestals are formed from a single piece);

**a plurality of leads** (leads 17 and 18) **each comprising an inner lead portion** (inner portion towards the die) **that extends to an outer lead portion** (outer portion furthest away from the die); **and**

**a first bond wire extending from the die to a first of the plurality of stamped pedestals** (bond wire 15), **and a second bond wire extending to an inner lead portion** (bond wire 22).

**Pritchard is silent with respect to explicitly disclosing that the plurality of leads are metallic, the second bond wire extends from the first of the plurality of stamped pedestals to the inner lead portion, and a**

**package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions.**

**Kwon discloses an integrated circuit structure** (e.g. figure 5), **comprising a first bond wire** (bond wire 160) **extending from the die** (die 154) **to a first of the plurality of pedestals** (pedestals 158), **and a second bond wire** (bond wire 162) **extending from the first of the plurality of pedestals to an inner lead portion** (inner lead portion of lead 156); **and a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions** (e.g. as seen in figure 5, there is a package, denoted by a dashed line, that encapsulates the die, paddle, wires and inner lead portions).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the second bond wire extends from the stamped pedestal to the inner lead portion since Pritchard discloses that electrical connections may be formed between the die, pedestals, and surrounding leads, and Kwon discloses that connections between pedestals and surround leads can be made. One would have been motivated to form a wire bond between the semiconductor die and the pedestal, and between the pedestal and the inner portion of the lead in order to relieve the wire bond of stress formed by making a direct connection between the semiconductor die and the inner portion of the lead.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that a package encapsulates the die, die paddle, inner lead portions, and bond wires since it was well known in the art that semiconductor structures are encapsulated in such a manner, as supported by Kwon. One would have been motivated to encapsulate the structure in order to protect the inner device elements from external stresses.

Furthermore, although Pritchard does not explicitly disclose forming the surrounding leads from metal, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the surrounding leads were formed from metal since Pritchard discloses connecting the leads to the die via wire bonds to form an electrical circuit, and it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use metal for the surrounding leads since it is electrically conductive, durable, and inexpensive.

b. Regarding claim 17, **Pritchard discloses an integrated circuit** (e.g. figure 1), **comprising:**

**a semiconductor die** (die 11);

**a carrier device comprising a planar surface onto which the die is attached** (paddle 16, disclosed in col. 1, line 65, which is the portion of leadframe 10 under semiconductor die 11), **where a plurality of stamped**

**pedestals** (pedestals 12 and 13, disclose in col. 1, lines 65 – 67 to be stamped) **are arranged on the carrier device exteriorly surrounding and adjacent to the planar surface** (e.g. as seen in figure 1, the pedestals 12 and 13 exteriorly surround and are adjacent to the top of the die paddle region under the semiconductor die 11), **where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure** (e.g. as seen in the figure, the carrier device, die paddle, and stamped pedestals are formed from a single piece);

**a plurality of leads** (leads 17 and 18) **each comprising an inner lead portion** (inner portion towards the die) **that extends to an outer lead portion** (outer portion furthest away from the die); **and**

**a first bond wire extending from the die to a first of the plurality of stamped pedestals** (bond wire 15), **and a second bond wire extending to an inner lead portion** (bond wire 22).

**Pritchard is silent with respect to explicitly stating that the carrier device and the plurality of leads are "metallic", and the second bond wire extends from the first of the plurality of stamped pedestals to the inner lead portion.**

**Kwon discloses an integrated circuit structure** (e.g. figure 5), **comprising a first bond wire** (bond wire 160) **extending from the die** (die 154) **to a first of the plurality of pedestals** (pedestals 158), **and a second bond**



**wire** (bond wire 162) **extending from the first of the plurality of pedestals to an inner lead portion** (inner lead portion of lead 156).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the second bond wire extends from the stamped pedestal to the inner lead portion since Pritchard discloses that electrical connections may be formed between the die, pedestals, and surrounding leads, and Kwon discloses that connections between pedestals and surround leads can be made. One would have been motivated to form a wire bond between the semiconductor die and the pedestal, and between the pedestal and the inner portion of the lead in order to relieve the wire bond of stress formed by making a direct connection between the semiconductor die and the inner portion of the lead.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use a metallic material in the carrier device of Pritchard, since Pritchard discloses connecting leads to the carrier device (stamped pedestals) to form an electrical circuit, and it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshin*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to make the carrier device metallic in order to create a conductive portion of the carrier to complete an electrical circuit, as well as allowing the pedestals to be formed easily by stamping.

Furthermore, although Pritchard does not explicitly disclose forming the surrounding leads from metal, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the surrounding leads were formed from metal since Pritchard discloses connecting the leads to the die via wire bonds to form an electrical circuit, and it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use metal for the surrounding leads since it is electrically conductive, durable, and inexpensive.

c. Regarding claim 2, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, as cited above, wherein the stamped pedestals have sidewalls with an angle ( $\alpha$ ) greater than 45 degrees with respect to a plane of the carrier device die paddle** (e.g. figures 1 and 3 of Pritchard show the angle of the pedestal sidewall has an angle of 90 (figure 1) and greater than 45 degrees (figure 3) with respect to the top or bottom plane of the die paddle).

d. Regarding claim 3, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, as cited above, wherein the stamped pedestals each have a plane surface which is parallel to a chip connection area plane of the carrier device** (e.g. as seen in figure 3 of Pritchard) **and each has an area for connection of a single bonding wire** (e.g. as seen in figure 1 of Pritchard,

there is an area surrounding the bond wire connection on the pedestals 12 and 13 for connecting a single bond wire 14 or 15).

e. Regarding claim 4, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, as cited above, wherein a height of each of the stamped pedestals lies in the range between 1/10 and 1.5 times the height of the semiconductor die** (as seen in figure 3 and disclosed in col. 2, lines 15 - 17 of Pritchard, the stamped pedestals have a height the same as the semiconductor die, and therefore are within the claimed range).

f. Regarding claim 5, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, as cited above, but is silent with respect to a height of each of the raised pedestals lies in the range from 1/5 to twice a material thickness (h) of the carrier device. Pritchard and Kwon show that the height of the pedestal may be about 0.5 times the height of the carrier device, but it is not explicitly stated.**

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that the pedestals are within the range of 1/10 to 2 times the height of the carrier device, since Pritchard and Kwon suggests through the figure this may be the case, and it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves

only ordinary skill in the art. *In re Aller*, 105 USPQ 233. One would have been motivated to make the height of the pedestal within the range of the carrier device in order to reduce lead length and stress on the leads.

g. Regarding claims 6 and 7, **Kwon discloses the structural limitations of the integrated circuit, as cited in claim 16. The process by which the raised pedestal is formed is not given patentable weight since the patentability of a product does not depend on the method of production. See MPEP 2113.**

h. Regarding claim 13, **Pritchard in view of Kwon discloses the integrated circuit of claim 17, as cited above, where the stamped pedestals make an angle ( $\alpha$ ) greater than 45 degrees with the plane of the carrier device at all sidewalls** (e.g. figures 1 and 3 of Pritchard show the angle of the pedestal sidewalls have an angle of 90 (figure 1) and greater than 45 degrees (figure 3) with respect to the top or bottom plane of the die paddle).

**Pritchard and Kwon are silent with respect to explicitly stating the sides have rounded junctions parallel to the plane of the carrier device or being rounded as a whole.**

However, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that the sides of the pedestals to have rounded junctions parallel to the plane of the carrier device or are rounded as a whole, since it has been held

by the courts that a change in shape or configuration, without any criticality, is nothing more than one of numerous shapes that one of ordinary skill in the art will find obvious to provide based on the suitability for the intended final application. See *In re Dailey*, 149 USPQ 47 (CCPA 1976). It appears that the disclosed device of Kwon would perform equally well shaped as disclosed by the Applicant. One would have been motivated to have rounded pedestals since materials deposited often have rounded edges due to the formation process.

i. Regarding claim 14, **Pritchard in view of Kwon disclose the integrated circuit of claim 17, as cited above, where the height of the stamped pedestals lies in the range between 1/10 of the die height and the die height itself** (as seen in figure 3 and disclosed in col. 2, lines 15 - 17 of Pritchard, the stamped pedestals have a height the same as the semiconductor die).

j. Regarding claims 22 and 23, **Pritchard in view of Kwon disclose the integrated circuit of claims 16 and 17, as cited above respectively, where a height of at least one of the stamped pedestals is between 1/10 of a height of the metallic carrier device to the height of the metallic carrier device** (e.g. as seen in figure 3 of Pritchard, the intersection of the stamped pedestals 23 with the die pad 21 has a height between 1/10 the height of the carrier device 16 and the height of the carrier device. Furthermore, it has been held that when the prior art discloses the general conditions of the claimed invention, discovering the

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optimum or workable ranges involves only ordinary skill in the art. See MPEP 2144.05).

k. Regarding claims 24 and 25, **Pritchard in view of Kwon disclose the integrated circuit of claims 16 and 17, as cited above respectively, where the metallic leads are separate from the metallic carrier device** (e.g. as seen in figure 1 of Pritchard, the leads 17 and 18 are separate from the carrier device 16) .

8. Claims 8 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Pritchard in view of Kwon, and in further view of Carter, Jr. et al. (US 6,365,976 B1, prior art of record).

a. Regarding claim 8, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, but are silent with respect to a silver or gold finish applied to the stamped pedestals.**

**Carter discloses that gold or silver finishes may be applied to raised pedestals in integrated circuits** (Col. 5, lines 18 - 22, disclose that the surface of the pedestals have a foil on them which may consist of silver or gold, or the pedestal may be covered with a tin-silver layer).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that there is a gold or silver finish on the raised pedestals since it was known in

the art that such pedestals in integrated circuits may have a finish applied to them, as disclosed by Carter. One would have been motivated to have a gold or silver finish applied to the pedestals since gold and silver promote the bonding of the wires to the pedestals and are highly conductive.

b. Regarding claim 15, **Pritchard in view of Kwon disclose an integrated circuit, but are silent with respect to only in the areas of the stamped pedestals, a finish, particularly silver or gold, is provided for bondability.**

**Carter discloses that areas of pedestals may be provided with a gold or silver finish** (col. 5, lines 20 - 22, discloses that the pedestal ("dimple") may covered with a layer of tin-silver).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that there is a gold or silver finish on the raised pedestals since it was known in the art that such pedestals in integrated circuits may have a finish applied to them, as disclosed by Carter. One would have been motivated to have a gold or silver finish applied to the pedestals since gold and silver promote the bonding of the wires to the pedestals and are highly conductive.

### ***Response to Arguments***

9. Applicant's arguments filed August 5, 2009 have been fully considered but they are not persuasive. In particular, the Applicant argues that the prior art of Pritchard

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teaches away from incorporating bonding wires of Kwon such that the pedestals are connected to the leads via the bonding wires. This is not found persuasive since nowhere in Pritchard is there disclosed that there cannot be bonding wires that connect the pedestals to the surrounding leads. The applicant asserts that Pritchard teaches away from connecting the pedestals to the leads because the *"wires may fracture and sag during temperature cycling and thermal shock"* (page 10 of Applicants remarks). However, Pritchard does not teach away from connecting the pedestals to the leads by using such reasoning. Instead, Pritchard discloses that the wires connecting the semiconductor die to the raised pedestal are done such that the wires *"will not sag and contact the die in an undesirable location"* (col. 2, lines 17 - 18). This statement does NOT preclude the connection of the pedestals to the surrounding leads by a wire bond. Rather, Pritchard shows that there indeed may be wire bonds directly connected to the surrounding leads (figure 1, wire bonds 22).

Secondly, the Applicant argues that Kwon teaches away from electrically interconnecting the pedestals (page 11 of Applicant's remarks), since the Applicant asserts *"Kwon teaches that the integrated circuit package 100,150 'uses an electrically-insulated, heat conducting substrate 102 as a bonding pad for an integrated circuit die...'"* (page 10 of Applicant's remarks). The Examiner submits that the properties of the substrate is not germane to the teaching relied upon for the combination of Kwon with Pritchard. Instead, the Examiner has used Kwon to teach the formation of multiple leads surrounding a semiconductor die, and the interconnection of the leads via wire bonds (as seen in figures 4 and 5 of Kwon). The leads are necessarily electrically



conductive since they could not conduct electrical signals and would not be wire bonded to each other and the integrated circuit unless they were electrically interconnected. Hence, it is the connection of the leads to the pedestals of Kwon that is used to modify the device of Pritchard, and not the material of the substrate.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Furthermore, it is submitted that the combination of the teachings of Kwon does not render the invention of Pritchard unsatisfactory for its intended purpose (see MPEP 2143.01). The Examiner has provided motivation to combine the teaching of the interconnections of the leads and pedestals that would have been obvious to one of ordinary skill in the art. It is well-known that interconnecting the leads and pedestals of Pritchard would be desirable based on the circuit structure of the semiconductor die and the external circuit to which the carrier device would be connected. Therefore, the Examiner maintains that the prior art of Pritchard in view of Kwon renders obvious the inventions of claims 16 and 17.

***Conclusion***

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/  
Primary Examiner, Art Unit 2892

/Robert Huber/  
Examiner, Art Unit 2892  
November 21, 2009